REMARKS

Present Status of the Application

The Office Action rejected claims 7 and 10 under 35 U.S.C. 102(b) as being anticipated by Brady (US-6,118,717, "Brady" hereinafter). The Office Action objected to claims 8 and 9 as being dependent upon rejected base claims, but would be allowable if rewritten in independent form.

Replacement drawings for FIG. 1 and FIG. 2 have been attached for overcoming the objections as identified in Items 3 and 4 of the Office Action dated October 24, 2005 on Page 2.

Applicants respectfully traverse the rejections addressed to claims 7 and 10 for at least the reasons set forth below.

Applicants also have amended claims 3 and 9 for improved compliance with the written description and enablement requirements of 35 U.S.C. 112, first paragraph, without the introduction of new matter.

Miscellaneous Issues

The change of claim limitation "preset voltage is one half of the voltage drop on the bit line" in claims 3 and 9 to "preset voltage is about one half of the voltage drop on the bit line" is implicitly or inherently supported in Paragraphs [0009], [0025], and [0026] of the present invention. For example, Paragraph [0026] describes that "...the pull-down

voltage of the bit line bar BLB is modifiable", which clearly implies that the voltage drop on the bit line does not have to be exactly one-half. Furthermore, since a person skilled in the art shall realize the physical difficulty of obtaining "exactly" one half of the voltage drop on the bit line to be the same as the preset voltage, the proposed amendment to claims 3 and 9 should allow for improved fullfillment of the enablement requirement of 35 U.S.C. 112, first paragraph.

Discussion of Objections

FIGs. 1-2 are objected to as failing to comply with 37 CFR 1.84(c) and 37 CFR 1.84 (a) as noted in Items 3 and 4, respectively, in the Office Action dated October 24, 2005. The drawings FIGs. 1-2 of the present invention are corrected in the form of "Replacement Sheets" and are attached herein.

In view of the aforementioned amendments, Applicants respectfully assert that the objections to Items 3 and 4 in the Office Action are no longer proper.

Claims 8 and 9 are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form.

Initially, it is noted with great appreciation that the Examiner considers the subject matter of claims 8 and 9 as being allowable over the art of record. In response thereto, the rejection to independent claim 7 has been traversed to make dependent claims 8 and 9 allowable. In view of the aforementioned, Applicants respectfully assert that the objections are no longer proper.

Discussion of the claim rejection under 35 USC 102

The Office Action has rejected claims 7 and 10 under 35 U.S.C. 102(b) as being anticipated by Brady (US-6,118,717, "Brady" hereinafter).

Applicants respectfully traverse the above rejections as set forth below.

In claim 7 of the present invention, the following claim limitation: "the reading operation comprising: charging the bit line and the bit line bar to a power voltage" is fully supported in FIG 5 **shown as VDD** and also in Paragraph [0022] in the present invention:

"In this embodiment, the bit line BL and the bit line bar BLB are charged to the **power voltage VDD**." As one can see, there is **no** "precharging to **Vdd/2**" found for the "reading operation" as claimed in claim 7 in the present invention.

On the other hand, col. 2, lines 30-33 in Brady describes the following: "... allow for **precharging of the nodes to a reference voltage, such as Vdd/2**, prior to a memory read ....." In addition, col. 2, lines 42-44 in Brady describes the following: " There exists equilibrate circuitry 165 in a conventional DRAM device that comprises ..... an EQ line 170, **a Vdd/2 line 175**...." Furthermore, col. 5, lines 35 – 45 in Brady describes the following: "To begin the read cycle, power to the sense amplifier 135 is turned off by applying a logic high and low voltage level to control lines SP 162 and SN 164, respectively. An equilibrate (EQ) signal 170 next transitions to a logic high voltage level prior to time T40 thereby equalizing and **precharging the bit line pair 110** and the nodes within sense amplifier 135. Once the **bit line pair 110** and sense amplifier 135 are **precharged** and equalized, the EQ line 170 is transitioned to a logic low voltage level at time T41. Next, the word line (WL) signal 115 transitions to a logic high voltage level at

time T42." As further illustrated by EQ 170 and **Vdd/2 175** in FIG. 1b in Brady, the Equilibrate Circuitry coupling to EQ 170 and **Vdd/2 175** for the transistors 185 in FIG. 3 in Brady, and the BIT LINES, EQ, WL with respect to T_{41} and T_{42} in FIG. 4 in Brady, the aforementioned "precharging of bit lines to **Vdd/2**" is fully described in Brady.

Furthermore, col. 8, lines 15-40 in Brady further describes the precharging of the bit line pair 110.

It is clearly evident that the reading operation in claim 7 of the present invention describes a charging **to VDD**, whereas, Brady teaches precharging **to Vdd/2** instead.

Furthermore, the BIT LINES, EQ, and WL in FIGs. 4 & 7 in Brady are clearly patentably distinguishable compared to FIG. 5 of the present invention.

In addition, Brady admittedly described in col. 6, lines 4-7 that "Because this read operation is not part of the present invention....." Therefore, the "reading operation" in claim 7 in the present invention is clearly patentable over Brady.

Finally, the waveforms in FIG. 2 in Brady which illustrate a traditional read-write operation are clearly patentably indistinguishable to those of FIGs. 4 & 7 of the read-write operations of the embodiments in Brady.

As a result, claim 7 is patentable over Brady and should be allowed.

If independent claim 7 is allowable over the prior art of record, then its dependent claim10 is allowable as a matter of law, because dependent claim 10 contains all the features of its respective independent claim 7.

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CONCLUSION

Applicants respectfully thank the Examiner for the allowance of claims 1-6. For at least the foregoing reasons, it is believed that all the pending claims 1-10 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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